**Amendment to the Specification:**

**Please amend the title of the present application as follows:**

A1

~~A High~~ Apparatus and Method for an Improved Performance VLIW Processor

**Please amend the paragraph, which begins on page 20, line 11, as follows:**

A2

In the present embodiment of the invention, the assembly code written for the VLIW processor consists of VLIW packets with one issue group having 64 bits and the other issue group having 48 bits. Thus, if a particular VLIW packet contains only one issue group, the VLIW packet is divided up into two issue ~~group~~ groups, with one issue group being 64 bits and the other being 48 bits. Moreover, the VLIW packets are not permitted to have three or more issue groups. Thus, in the present example, all VLIW packets processed by the invention's VLIW processor 300 would contain exactly two issue groups, one issue group being 64 bits and the other issue group being 48 bits. The unique architecture and the unique issue grouping in the present invention results in a doubling of the execution speed of the VLIW process as explained above. However, as discussed below, this doubling of the execution speed does not result in a doubling of the consumed power. As such, the present invention significantly differs from prior attempts to increase the processing speed of conventional VLIW processors.

**Please amend the paragraph, which begins on page 22, line 16, as follows:**

A3

In contrast, according to the present embodiment of the invention, during each clock cycle, a new VLIW packet is being fetched. For example, during execution of issue group 422 of VLIW packet 410 and issue group 442 of VLIW packet 430 in the first clock cycle, a new VLIW packet is fetched which would be executed after completion of the execution of VLIW packets 410 and 430. Similarly, during execution of issue group 424 of VLIW packet 410 and issue group 444 of VLIW packet 430 in the second clock cycle, another new VLIW packet is fetched which would be executed after completion of the execution of VLIW packets 410 and 430. Thus, during the third and fourth clock cycles, both ~~the~~ VLIW packets which were fetched during the execution of VLIW packets 410 and 430 would be executed. It is thus manifest that any circuitry that is clocked during execution of the various issue groups in the present embodiment of the invention, for example the fetch and decode logic units in the VLIW processor, would be efficiently utilized and power would not be needlessly consumed.